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# Multi-Cell Soft Errors at the 16-nm FinFET Technology Node

N. Tam<sup>1</sup>, B. L. Bhuv<sup>2</sup>, L. W. Massengill<sup>2</sup>, D. Ball<sup>2</sup>, M. McCurdy<sup>2</sup>, M. L. Alles<sup>2</sup>, I. Chatterjee<sup>3</sup>

<sup>1</sup> Marvell Semiconductor, San Jose, CA, <sup>2</sup> Vanderbilt University, Nashville, TN 37212 USA, <sup>3</sup> University of Bristol, Bristol, UK  
ntam@marvell.com

**Abstract**—Soft error performance of 16-nm FinFET SRAM designs fabricated using a commercial bulk CMOS process is evaluated using heavy-ions. Results included supply voltage variations show that multi-cell upsets dominate soft-error rates. Dual-port SRAM has higher cross-section than single-port SRAM but did not have any multi-cell upset across the bit-line direction. TCAD simulations showing the extent of the perturbation in the electric parameters as a function of particle LET support the experimental data.

**Keywords**- SRAM, FinFET technology, scaling, soft errors, TCAD modeling, multi-bit upsets

## I. INTRODUCTION

With the conversion from planar to FinFET transistor structure for advanced technology nodes completed in the recent past, the focus has shifted to reliability of FinFET technologies. For planar technologies, soft-error (SE) related failures were expected to have the highest FIT rates compared to any other type of failures [1]. The 3-D structure of FinFET transistors, as opposed to 2-D structure of planar transistors, is expected to alter the charge generation and collection processes associated with soft errors [2]. Available data and models for FinFET SRAM and flip-flop designs show a decrease in overall soft-error rates (SER) as shown in Fig. 1a and 1b [2,3]. Fig. 1(a) shows the experimental results for multiple technologies spanning almost a decade. All bulk planar technologies show a declining trend as feature size is reduced on an IC. At the introduction of FinFET technology node, a sharp drop in SER is observed. The drop in SER is significant, but less than a decade. Similarly, simulation results, shown in Fig. 1(b), show the differences between a planar and FinFET technology for collected charge after a single-event ion hit. The 3D physical structure, along with the narrow connection to the substrate for FinFET yields significantly less collected charge than their bulk counterpart under identical conditions. All these results point to the superior performance of FinFET node for SER over comparable bulk node.

However, FIT rates (or collected charge after an ion hit) alone do not give a complete picture of SRAM SER vulnerability. With the close proximity of transistors in an SRAM design, multi-cell upsets are fast becoming the norm. In this paper, all multi-cell upsets, whether they are across columns or across rows, are termed as Multi-Cell Upsets (MCU). As the extent and range of MCU's across columns determine the interleaving and MCU's across rows determine error correction and detection (ECC) parameters used by designers, it is fast becoming a very important test for all SRAM designs. To reduce the risk of having multi-bit upset in an ECC protected word due to MCU, larger interleaving distance is required which could incur area, power, and

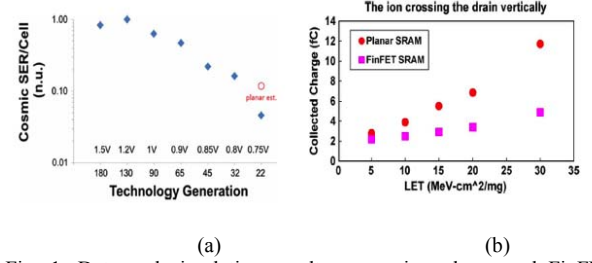


Fig. 1. Data and simulation results comparing planar and FinFET technologies [2,3].

performance penalties. Designers may end up using non-optimum aspect ratio for the layout of the array resulting in either increased FIT rates or decreased performance for SRAM designs. With the ECC and interleaving techniques widely adopted by the industry to mitigate soft errors, it is important to measure the spread of these errors so as to determine the best design parameters to meet reliability requirements. In this paper, the overall upset rates as well as single-bit and multi-cell upsets are investigated for a 16-nm bulk FinFET SRAM design from a commercial foundry using heavy-ions of varying Linear Energy Transfer (LET) values for different supply voltages. Single-port and dual-port SRAM designs were investigated. Results show that MCU's dominate for high-energy particles, and that the range of MCU's may span over 4 columns or 6 rows for particles with high LET values at reduced supply voltages.

## II. TEST CIRCUITS & EXPERIMENTS

Test ICs were fabricated at a commercial foundry using a 16-nm bulk FinFET process. SRAM designs tested were single-port and dual-port designs. The nominal supply voltage for SRAM ICs is 900 mV. The supply voltages used for tests were 600 mV, 700 mV, 800 mV, and 900 mV. Tests were carried out with all\_0, all\_1, and checkerboard patterns. All tests were conducted in air, at room temperature, at normal incidence. Heavy-ion tests were performed at Lawrence

TABLE I  
16 MeV/Nucleon Cocktail Components

Ion	Energy (MeV)	LET (MeV/mg/cm²)	Range <sub>final</sub> (µm)
<sup>14</sup> N	234	1.16	508
<sup>20</sup> Ne	321	2.4	348
<sup>29</sup> Si	452	4.35	274
<sup>40</sup> Ar	642	8.34	256
<sup>63</sup> Cu	1007	16.53	190
<sup>78</sup> Kr	1226	24.98	163
<sup>124</sup> Xe	1955	49.29	147

Berkeley National Laboratory (LBNL) using 16 MeV/nucleon cocktail. The range of particle LET's used was 1–50 MeV-cm<sup>2</sup>/mg. Table I lists the ion beams, the corresponding energy, LET values and the ranges of these ions in Si [4].

During testing, SRAM cells were written to once and then continuously read from. Whenever an error was read, correct data was written back into the memory cell. All errors that were adjacent physically and temporarily to each other (across columns or rows) were treated as multi-cell upsets. The address for each upset bit was also recorded to verify adjacency for multi-cell upsets. Data were processed after the experiment to determine the size of multi-cell upset clusters. Upset cross-sections were calculated by

$$\text{Cross Section} = \frac{\text{total \# of errors}}{\text{size\_of\_memory\_array} * \text{fluence}} \quad (1)$$

### III. RESULTS

Experimental cross-section per bit values for different values of supply voltage and particle LET for single port designs are shown in Fig. 2. Curves in Fig. 2 (and all other figures) were generated using all upsets, single-bit upset (SBU) and MCU. The threshold LET value (the LET value at which upsets start to appear upon exposure) is less than 1 MeV-cm<sup>2</sup>/mg. Some upsets were also observed at 600 mV supply voltage for He ions with an LET value of 0.105 MeV-cm<sup>2</sup>/mg. Particles with an LET value of 0.105 MeV-cm<sup>2</sup>/mg deposit approximately 0.001 pC/um of charge during an event. The fact that the SRAM cell was upsetting even at such low values of deposited charge indicates a very low critical charge for the SRAM cell. Specifically, these SRAM cells may be vulnerable to upsets due to muons, low-energy protons, or high-energy electrons [5-7]. If the SRAM vulnerability to these particles is confirmed, it may significantly increase the FIT rates for terrestrial operations.

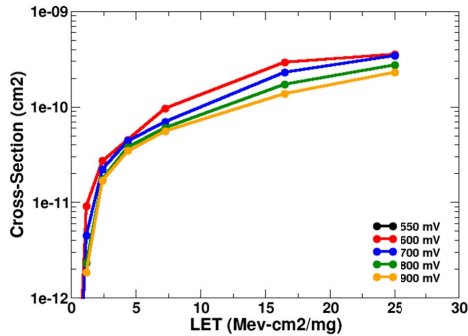
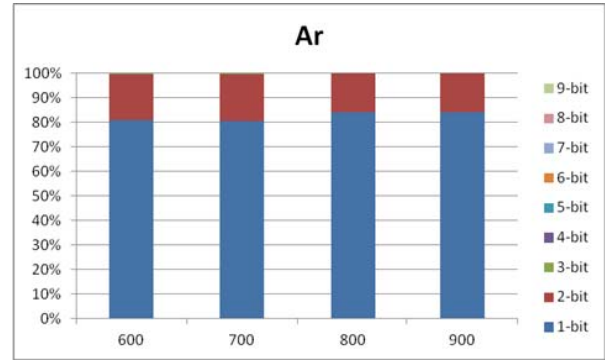


Fig.2. Upset cross-section per bit vs. particle LET for the single port SRAM design at different supply voltage values.

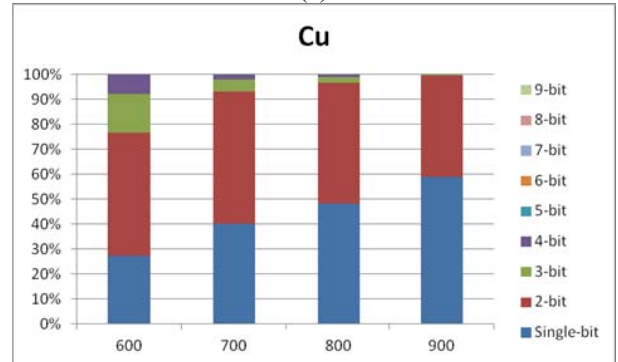
Cross-section values have historically shown Weibull shape when plotted as a function of particle LET values. The main data points of interest to the radiation effects community is the threshold LET values at which the upsets start to appear – an indication of critical charge value for the SRAM cell, and the saturated cross-section values indicative of the sensitive area for an SRAM cell. Saturated cross-section values for high LET particles usually saturate indicating limited sensitive area for a given SRAM cell. However for 16-nm SRAM design,

the cross-section values do not seem to saturate as particle LET increases. One of the reasons for this behavior is that the cross-section values plotted includes single-bit and multi-cell upsets. As particle LET increases, the increased number of MCU keeps increasing the total number of upsets, resulting in non-saturation of cross-section curve. For the designs tested in this work, the cross-section values do not seem to saturate even at an LET of 50 MeV-cm<sup>2</sup>/mg.

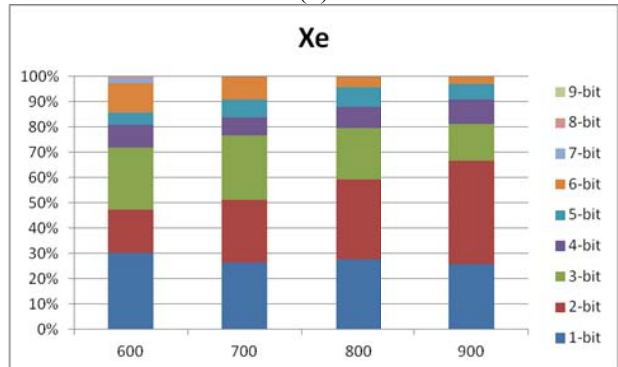
Cross-section curves, shown in Fig. 2, do convey the SRAM vulnerability to soft errors, but designers still need to know the extent of MCU. For advanced technology nodes, as indicated earlier, the extent of MCU along the rows and columns determines the ECC and interleaving parameters. Fig. 3 shows the relative contribution to overall SER for different MCU values. MCU's are caused when multiple SRAM cells collect



(a)



(b)



(c)

Fig. 3. Relative contribution of SBU and MCU as a function of supply voltage for different particle LETs for 16-nm SRAM.

more than critical charge for a single ion hit [8-9] (this is usually referred to as charge-sharing). The extent of MCU (the number of upset bits) represents the distance over which charge may diffuse and get collected by multiple SRAM cells. Fig. 3(a) shows the MCU contribution for Ar with an LET value of 7.27 MeV-cm<sup>2</sup>/mg. For this particle, the maximum number of multiple-upset bits is 2. With the SRAM cell size at the 16-nm node expected to be 0.05-0.07  $\mu\text{m}^2$ , 2-bit MCU at this LET yields a good estimate of the distance over which enough charge may get collected to cause an upset. As particle LET increases to 16.5 MeV-cm<sup>2</sup>/mg for Cu, as shown in Fig. 3(b), the highest number MCU increases to 4. Further increases in LET for Xe (LET = 49 MeV-cm<sup>2</sup>/mg) increase the number of MCU bits to 8. These results show that significant amount of charge being collected by multiple transistors from a single incident particle for FinFET technologies. These results clearly show that charge-sharing effects are not diminished at the 16-nm FinFET technology node.

The supply voltage dependence in Fig. 3 shows increased number of occurrences for large cluster sizes as supply voltage is decreased. In addition, the MCU cluster size also increases with reduced supply voltage. The increase in MCU cluster size is a direct result of the decreased critical charge as supply voltage is reduced. The reduced power supply will result in reduced  $Q_{\text{crit}}$  for SRAM cells, resulting in more cells vulnerable to an ion hit. All SRAM cells surrounding the hit location will collect charge as a result of charge deposition. As the amount of charge collected by a cell is a weak function of supply voltage, the collected charge value does not change significantly as supply voltage is reduced. The reduction in  $Q_{\text{crit}}$  due to supply voltage reduction is the primary cause for the increase in the number of upset cells. For a given technology node, the parameters controlling charge diffusion in the substrate after an ion strike are independent of supply voltage. As the charge collected by a node due to diffusion process is a weak function of the nodal voltage [9], charge collected by SRAM cells surrounding the hit location is mostly constant when supply voltage is varied. One of the major effects of reduced supply voltage is reduced critical charge. This reduction in critical charge increases the number of SRAM cells that have collected more than critical charge after an ion hit, resulting in increased cluster size as seen in Fig. 3.

Results for cross-section per bit as a function of particle LET for different supply voltages for dual-port SRAM design are shown in Fig. 4. Cross-section values for particles with high LET also show a non-saturating behavior. This is again caused by the inclusion of MCU in the overall error numbers. As the particle LET increases, the number of MCU increases, resulting in increasing cross-section per bit. Similar to single-port SRAM designs, the threshold LET values for the SRAM cell is very low. In fact, the threshold LET values for both types of memory cells are indistinguishable from the test results. Cross-section curves for single-port and dual-port

designs for 800 mV supply voltage clearly show similar threshold LET, as shown in Fig. 5.

Dual-port SRAM cells are usually designed with two sets of access transistors allowing access to the SRAM cell data on two different bit lines. The increased number of access transistors increases the nodal capacitances associated with the storage nodes. With increased capacitance, the critical charge required to cause an upset also increases. For a first order of approximation, the critical charge is proportional to  $V_{\text{dd}} * C_{\text{node}}$ , where  $V_{\text{dd}}$  is the supply voltage and  $C_{\text{node}}$  is the nodal capacitance for the storage node. Accordingly, the dual-port SRAM cells are expected to have higher critical charge than single-port SRAM cells, resulting in higher threshold LET and lower saturated cross-section values than single-port SRAM cells. The lack of distinction between these two designs for threshold LET values stems from the very low critical charge for both the cells. For the particle LET values used in this study, the amount of charge deposited is much higher than the

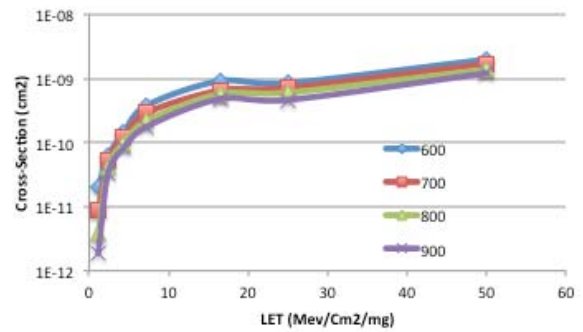


Fig. 4. Cross-section results for dual-port SRAM designs as a function of supply voltage.

critical charge for each cell. As a result, a small increase in critical charge due to increased nodal capacitances is overcome by the large amount of charge deposited by the particles used in the tests.

Saturated cross-section values for storage cells are indicative of the sensitive area for all vulnerable transistors. For older technologies, this used to be the drain regions of all vulnerable transistors as ion hits outside the drain regions did not result in significant charge collection at circuit nodes. With the critical charge values at these technologies significantly higher than the amount of charge collected from ion hits outside the drain region, sensitive area (or saturated cross-section values) was obtained by adding drain area for all vulnerable transistors. For advanced technologies, very low critical charge means ion hits outside the drain regions are capable of causing an upset. As a result, sensitive area for a transistor extends beyond the drain area of a transistor. Usually, as critical charge increases, this sensitive area decreases due to the fact that collected charge is inversely related to the distance between the drain boundary and the hit location.



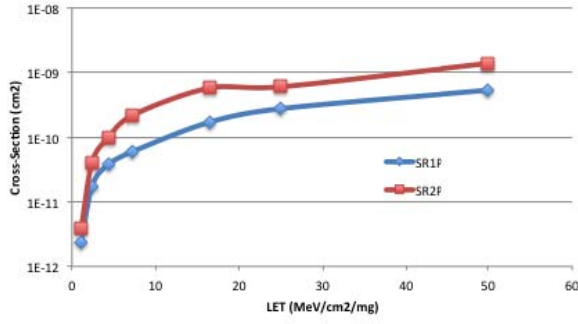


Fig. 5. Cross-section curves for single-port and dual-port SRAM designs for 800 mV supply voltage show very little difference in threshold LET values.

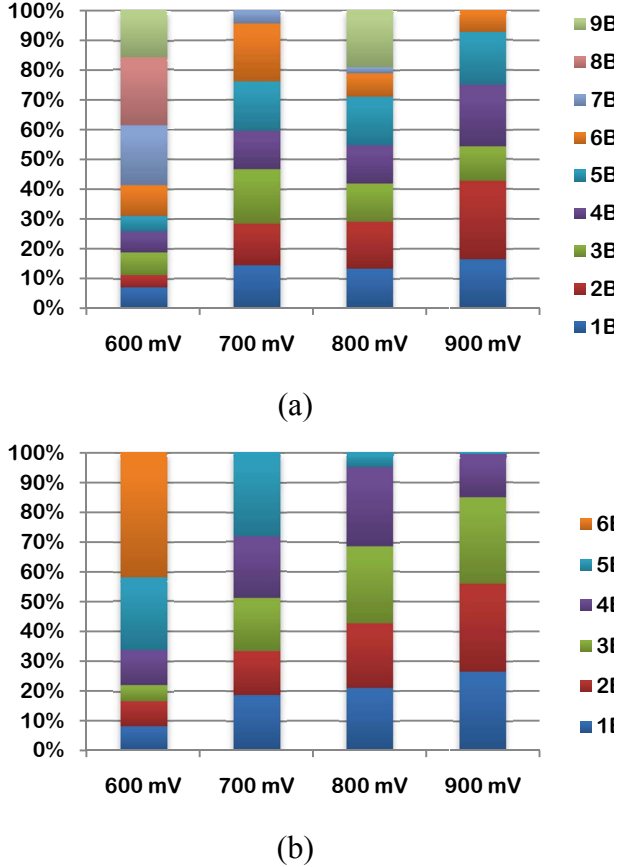


Fig. 6. MCU cluster size distribution for (a) single-port and (b) dual-port SRAM designs.

For dual-port SRAM design, the increased critical charge should result in decrease sensitive area and subsequently, lower saturated cross-section values compared to single-port SRAM designs. However, as Fig. 5 shows, dual-port SRAM designs have higher cross-section values than single-port SRAM designs. This is again due to the very low critical charge values for these SRAM cells. Increase in critical charge values for dual-port SRAM cell is not significant, as evidenced by curves in Fig. 4 and 5. Any decrease in sensitive area due to increased critical charge, as a result, is also going to be not significant. But the increased number of vulnerable transistors increases the total sensitive area per SRAM cell, resulting in significant increase in saturated cross-section

values as seen in Fig. 5. These results indicate that low critical charge values are the main determinants of the SER for these SRAM cells. Since increases in nodal capacitances or increases in transistors currents (both are effectively used for hardening flip-flop and logic circuits) need to be minimal to keep performance penalty reasonable, these approaches do not significantly affect the critical charge. As a result, the LET threshold values do not change significantly, but saturated cross-section values increase due to increased size of the SRAM cell. Designers need to be careful to avoid these approaches which increase the cell area without significantly affecting the critical charge.

Even though error cross-section values for dual-port SRAM design were higher than those for single-port SRAM design, MCU cluster sizes for dual-port SRAM design were smaller than those for single-port SRAM design. MCU data for dual-port SRAM design showed similar trends as those for single-port SRAM designs as a function of supply voltage and particle LET values. For example, for Xe ion with an LET value of 50 MeV-cm<sup>2</sup>/mg, the single-port SRAM designs showed up to 9-bit MCU (Fig. 3(c)) whereas dual-port SRAM designs showed up to 6-bit MCU. Fig. 6 also shows the relative contribution of each size of MCU cluster to the overall number of errors. For a given cluster size of MCU, the number of occurrences is smaller for dual-port SRAM designs compared to single-port SRAM designs. The main reason for this observation is the SRAM cell size. For dual-port SRAM designs, the size of the SRAM cell has similar height (i.e. in the row direction) as the single-port SRAM but the width (i.e. in the bit-line direction) is about twice as wide. As a result, the spread of charges in the row direction should be similar between the SRAM designs. But the spread of the charge across bit-line direction as indicated by the experimental results to be significantly impaired by the additional ports.

Table II shows the maximum cluster size across rows and columns for a given supply voltage. Since the SRAM cell layout is optimized to reduce charge sharing across the columns, the size of the cluster across rows is bigger than that across columns. Errors across rows indicate multiple words being affected, while errors across columns indicate multiple bits within a word being affected. MCU clusters for dual-port SRAM designs did not spread across the column direction, i.e. all MCU clusters for were confined to just one column. As a result, bit-interleaving requirement for dual-port SRAM designs does not need to be as restrictive as those for single-port SRAM designs at this technology node. Finally, for

TABLE II.  
Maximum size of the cluster across columns or rows

Supply Voltage	Single-Port		Dual Port	
	Max Row	Max Column	Max Row	Max Column
600 mV	30	3	6	1
700 mV	6	3	5	1
800 mV	5	4	5	1
900 mV	14	3	4	1

single-port SRAM designs, the cluster size of 14 and 30 was observed only once, while most of the cluster sizes for rows were less than 6

#### IV. TCAD ANALYSIS

Synopsys 3D TCAD simulations were carried out to estimate the extent of distance over which significant single-event effects (perturbation in electric potential, collected charge as a function of distance, etc.) occur in a structure representative of a 16 nm bulk FinFET technology. Simulations were run for single event strikes into the N-WELL, near the OFF-PMOS FinFET devices. This strike location was chosen because of the impact that single-event strikes have on de-biasing an N-WELL in a bulk CMOS process. Simulations were carried out for the nominal supply voltage of 0.9 V. In Fig. 7, the 2-D cross-section cut along the length of the N-WELL shows the electron density at 300 ps after a single event strike with LET=60 MeV-cm<sup>2</sup>/mg. At 300 ps after the ion strike, the electron density is  $4 \times 10^{19}$  cm<sup>-3</sup> in the vicinity of the hit location and stays above  $2 \times 10^{18}$  cm<sup>-3</sup> approximately 500 nm from the hit location. To put that dimension into perspective, a FinFET device is on the order of 100 nm at its largest point. For an SRAM cell size of  $\sim 0.039$   $\mu\text{m}^2$ , perturbation over such a wide distance will result in multiple bits affected in the SRAM array.

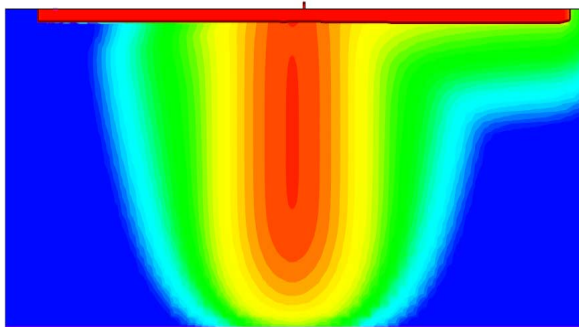


Fig. 7 Electron density at 300 ps after an ion hit with LET value of 60 MeV-cm<sup>2</sup>/mg. The small notch in the middle is an SRAM cell and the ion hit was located 500 nm on the left of the SRAM cell.

Simulation results, shown in Fig. 8, show the distance over which potential perturbations are observed with increasing particle LET. The figure shows the electrostatic potential through a doped n-type region (the higher than supply voltage potential shown on the chart is the result of the TCAD

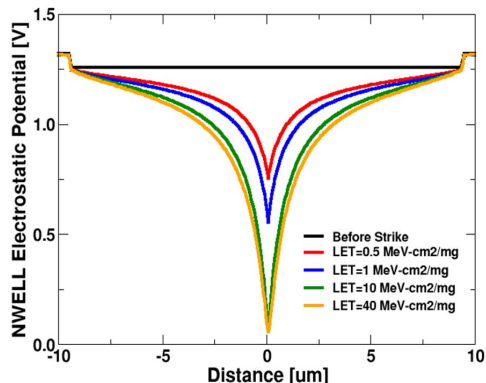


Fig. 8. Extent of electrostatic potential disturbance in an NWELL after an ion strike on an SRAM cell in the 16-nm FinFET node.

simulator characteristics. It is not the same as the externally applied supply voltage). Larger physical range of perturbations will result in increased number of cells affected by a single-ion hit. In Fig. 8, it is shown that the N-WELL electrostatic potential is greatly perturbed for several microns on either side of an ion strike when compared to a pre-strike condition.

#### V. CONCLUSIONS

Heavy-ion exposures for 16-nm FinFET SRAM show that SER is dominated by MCU's for high LET particles. Dual-port SRAM has higher cross-section than single-port SRAM but it should have more relaxed bit-interleaving requirement than the single-port SRAM. For a particle LET of 50 MeV-cm<sup>2</sup>/mg, the MCU cross-section is an order of magnitude higher than SBU cross-section. TCAD results show the extent of charge-sharing at this technology node. Results presented in this paper will help designers estimate the ECC and interleaving design parameters for FinFET SRAM designs at the 16-nm FinFET node.

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